**OxM Fast Track (FTx)**

**At-Scale Validation Requirement**

**Revision v2.1**

**Intel Taiwan At-Scale Validation Team**

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# **Revision Control**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Modifier** | **Date** | **Change Summary** |
| V1.0 | ASV TWN | 03/04/2022 | Initial release |
| V1.1 | ASV TWN | 03/16/2022 | * Made some minor updates * Add more specific requirement of test entry in section 1.5. |
| V1.2 | ASV TWN | 03/18/2022 | * Add BIOS configurations for TDX in section 2.1.4 Virtualization – Kata. * Add Gramine preprocess in 2.2.15. * Update section 2.1 test overview * Section 2.2, adding more test contents for extensive phase * Section 2.3, Baseline HW Material Requirement * Section 2.4, Pre-sighting management |
| V2.0 | ASV TWN | 05/09/2022 | V2.0 Release |
| V2.1 | ASV TWN | 12/08/2023 | * Add triage and debug process * Keywords of queries from Kibana/Elastic * Entry and exit criteria * Separate ASV test content out * Add contents related to data analysis |

# **Document Reviewers/Approvers**

|  |  |  |
| --- | --- | --- |
| **Area/Function** | **Representative** | **Role** |
| Intel ASV TWN Manager | Lin, River | Reviewer |
| Intel ASV Director | Gonzalez, Ricardo A | Approver |

# **Fast Track (FTx) Validation Framework**

The Fast Track (FTx) Validation Framework exists to document the core activities, main timeframe and roles within Intel ASV Team and OxM working model. The goal of the Framework is to drive consistency and repeatability in the performance driven across various Intel internal and external teams.

## **FTx Program Memorandum of Understanding: INTEL - OxM​**

The Fast Track program is designed to enable Original Design/Equipment Manufacturers ("OxM") to increase the value they provide to the end customers by offering improved hardware performance, reliability, and security. The Fast Track program model involves deep engineering collaboration between Intel and OxM to perform at-scale validation on OxM-constructed testbeds (“clusters”), optimize select workloads, and develop targeted solutions with increased performance and quality for scale to Next Wave (“NW”) CSP and CoSP end customers.”​

**Goals for At-Scale Validation**

* Improving at-scale hardware (CPU + Platform) quality and reliability
* Obtain/analyze telemetry (Si data) from clusters. Intel will need access to telemetry data generated for At-scale testing.
* Solve platform and CPU issues, help customers/partners build better platforms
* Help mitigate risks perceived by final customers for adoption of OxM server platforms

## **IS/IS NOT**

|  |  |
| --- | --- |
| IS | IS NOT |
| Black box testing | White box testing |
| System validation with datacenter scale sample size | Validation on single unit |
| At-Scale validation through cluster | Platform functionality and compatibility verification |
| Perform 3rd party stress tools as stressors | Benchmark/Performance verification |
| Debug methodology through cluster >=90% | Test scripts and images delivery by Intel ASV Team |
| Test requirement and training delivery by Intel ASV Team |  |
| Discover potential pre-sightings through FTx validation |  |

## **FTx Validation Timeframe**

Below timeframe provides an overview of what activities take place for OxM FTx Validation.



Here are the breakdown items of FTx Validation timeframe for each test phase with rough estimated test time. The validation planning from OxM should include the activities below but not limited, the actual plan can be adjusted based on resource, schedule or scope perspective.

1. **Training and Cluster Enablement – 4 weeks**
   * Training topics will be provided by Intel ASV Team
     + At-Scale cluster framework training
     + Container Orchestration
     + Data collection - In-band index queries
     + Data collection - OOB index queries
     + Docker Containerization
     + Telemetry usage
   * Cluster Enablement by Intel Infra Team
     + Admin Rack Architecture
     + Prometheus/Grafana
     + Elastic/Kibana
     + KAFKA
     + Logstash
     + Docker Registry
2. **Validation Enablement and Acceptance Test – 2 weeks**
   * Topics of validation enablement for each test phase
     + Docker containerization readiness
     + Test content and test plan identification
     + Cluster readiness verification
     + Gitlab/Github repo
     + Pipeline creation on Jenkins
     + Test plan reviewing
     + BKC/FW/SW/OS/Kernel/Driver/Tool level confirmation for phase entry
   * Acceptance Test and Trial-run
     + Trial-run with smaller sample size to check test content and environment readiness
     + Acceptance Test pass rate must be 100%
3. **FTx Validation – 3 weeks**
   * Test plan execution
   * Pre-sightings submission and clarification
   * Weekly meeting
   * Test reporting
4. **Bug Fix and Regression – 2 weeks**
   * Reserve for fixing MUST FIX pre-sightings
   * Regression test for code changing and fixes verification

## **FTx Roles & Responsibilities (R&R)**

The Roles and Responsibilities (R&R) of FTx validation for both Intel At-Scale Validation (ASV) Team and OxM are summarized below. Additional details are listed later in this section.

|  |  |
| --- | --- |
| Intel ASV Team | OxM’s Validation Team |
| The point of contact to OxM’s validation teams for a FTx project | The point of contact to Intel ASV Team for an assigned FTx project |
| Test requirement delivery and support test planning for OxM | Review test requirements and provide feedback to Intel ASV Team |
| Training of FTx validation topics arrangement for OxM | Attendees of trainings and request additional training topics if needed as well as perform acceptance test on OxM’s platforms |
| Milestone control | Milestone negotiation and achievement |
| Pre-sightings status tracking | Pre-sightings submission and management |
| Technical focal point of Intel external teams for FTx validation topics | Technical focal of Intel ASV Team for FTx validation topics |
| Provide guidance/input to the OxM from validation perspective | Raise needed help to Intel ASV Team from validation perspective |
| Review OxM’s test plans and results | Provide test plans and test reports |
| Review OxM’s test resources and capabilities readiness | Arrange sufficient resources and capabilities for FTx validation |

**Intel ASV Team R&R**

The Intel ASV Team acts main contact windows across Intel internal and external validation teams. The responsibilities center around test planning, training and technical supporting for the OxM.

* The point of contact to OxM’s validation teams for a FTx project
* Test requirement delivery and support test planning for OxM
* Training of FTx validation topics arrangement for OxM
  + ASV Cluster
  + Container orchestration
  + Data collection – IB & OOB
  + Containerization
  + Telemetry
  + Jenkins and Gitlab library
  + Data Analysis and Cluster Stability
* Milestone control
* Pre-sightings tracking
* Technical focal point of Intel external teams for FTx validation topics
  + Kubernetes, Cluster and telemetry applications
  + Docker containerization
  + FW related troubleshooting and debugging
  + System Health Check (SHC) tool
  + 3rd party stress tools on I/Os
  + Performance and benchmark tools
  + Reliability, Availability and Serviceability (RAS) function
  + Virtualization applications
  + Software Guard Extensions (SGX)
* Provide guidance/input to the OxM from validation perspective
* Review test plans and results from OxM
* Review test resources and capabilities readiness from OxM

**OxM R&R**

In order to make FTx validation tasks successfully and smoothly, the engineers from OxM validation team must fit into one or more the following roles including Validation Lead, Test Execution Engineer and Subject Matter Experts.

Validation Lead

The OxM’s Validation Lead is responsible for the FTx validation management of planning, execution and data reporting.

* The point of contact to Intel ASV Team for an assigned FTx project
* Test requirement reviews and provide feedback to Intel ASV Team
* Request training topics if needed
* Provide test plans for reviewing
* Test status reporting
* Resources management
* Milestone negotiation and achievement
* Pre-sightings submission and management

Test Execution Engineer

The Test Execution Engineer performs test execution and record test results as well as discovering pre-sightings.

* Test plan execution
* Test results recording
* Pre-sightings discovery

Subject Matter Expert (SME)

The Subject Matter Experts (SMEs) are the OxM’s technical focal who are responsible for technical discussion with Intel ASV Team to ensure OxM’s validation team has the tools and knowledge to perform testing in FTx validation.

* Technical focal point for a project
* Technologies of FTx validation research
* Triage key pre-sightings
* Provide technical feedback to Intel ASV Team based on test requirement
* Provide test methodologies of each test content
* Areas of specification include
  + Kubernetes, Cluster and telemetry applications
  + Docker containerization
  + Platform specific subjects including HW, BIOS, BMC (IPMI, Redfish) etc.
  + 3rd party stress tools from I/Os perspective
  + Performance and benchmark
  + Reliability, Availability and Serviceability (RAS) function
  + Virtualization applications
  + Software Guard Extensions (SGX)

## **FTx Validation Entry/Exit Criteria**

The At-Scale Validation team owns the milestone control for all test phases which is responsible for ensuring all of necessary requirements to enter/exit a test phase are met before declaring entry or exit. For each test phase, below is the set of defined criteria that must be met for test entry or exit.

**FTx Validation Test Entry Criteria**

The process by which OxM/ASV team declares readiness to begin is called FTx Validation Test Entry. The test entry criteria consist of 13 items:

|  |  |  |
| --- | --- | --- |
| No. | Criteria | Description |
| 1 | Cluster Power On | All tasks completed per power on plan or infrastructure readiness plan. Systems delivered and proven capable to execute orchestrated validation execution and telemetry functionality meets expected tracking and monitoring requirements per failure criteria |
| 2 | Platform BKC | Alignment with platform BKC is completed. BKC transitions happen on all external releases (minimum requirement). Specific ingredient transitions in off-cycle mode are possible upon agreement with platform and BKC team to ensure risks are understood |
| 3 | Silicon availability | Cluster infrastructure team has plans to enable minimum counts of CPUs necessary to cover HW and platform milestones per product life cycle documentation and validation plan schedule. Item tracked as part of cluster power on milestones. |
| 4 | Content quality and execution method | Content must meet stability requirements per the power on phases. All content execution is completed with automated orchestration and meets ‘Test Anything Protocol’ to ensure telemetry is integrated into the test pass/fail monitors. |
| 5 | Cluster fleet stability | Calculation methods and tools for stability assessments are ready on first validation cycle and minimum failure criteria exists and meets the expected minimum measurement required for first UPLC criteria, i.e. component ES2 and/or Platform Beta. |
| 6 | Telemetry readiness | Proof of readiness is demonstrated at minimum against n-1 technology, i.e. reference SPR/EGS telemetry must have at least the same capabilities are those that currently exist in Whitley platform. Especially the path of uEFI debug logs through SOL (Serial-Over-LAN) and sensor list (via IPMI/Redfish) need to be feature completed and validated by the OxM. |
| 7 | OxM's SIT test report and known issues availability | OxM's SIT test should be completed and results should be reported prior to FTx Validation Entry. Any known pre-sightings will have been recorded for the product. Any pre-sightings that will not be resolved prior to test Entry must have been reviewed to ensure they will not block FTx testing.  An SI corner case configuration list (High speed interface) is required as well. |
| 8 | OxM's product is at least DVT level (HW & FW) | The FW and HW features of OxM’s product must be DVT level (HW feature enablement completed) at least and have been tested prior to test Entry. Especially, ACD and ASD function must be tested and functional. |
| 9 | Materials (UUTs, test tools) readiness | OxM's lab infra, configuration of test systems, AVL/CCL, and test tools must all be available and reviewed prior to test entry. Shipping configs of CSPs must be considered as validation configs first and get aligned between Intel and OxM. Unsupported parts (not in customer’s AVL/CCL) are not recommended. |
| 10 | Manpower readiness | All planned execution personnel must be available. All required training Intel provided for the project should be completed before test entry. |
| 11 | Acceptance test 100% passed | OxM will perform a set of ASV team defined acceptance tests to ensure that the systems and infrastructure are ready for test entry. Results with 100% passed will be provided to Intel ASV team prior to test entry. |
| 12 | All test plans ready and reviewed | The test Plans must be finalized and reviewed prior to test entry. |
| 13 | OxM’s pre-sighting list is provided and reviewed | OxM must provide the defect list to ASV team for reviewing to ensure no potential rick gating FTx validation progress prior to test entry. |
| 14 | Data analytics readiness | 1. OxM must maintain the correctness of data and logs inside the following indices.    1. qpool-\* (In-band logs)    2. sol-\* (OOB logs)    3. eventlog-\* (Event logs, including different types of system event logs from FW/OS/BMC from different sources to indicate system health/status)    4. crachdumps-\* (Crachdumps logs)    5. other relevant indices 2. OxM must maintain the correctness of failure keywords in [Appendices D](#_Appendices_D_–). 3. OxM must label the status of the SUT according to the status of the tests. (Execution, Debug, etc.) |
| 15 | Auto log collection after crash dump (ACD) | Systems must be able to collect logs after crash automatically through ACD. In addition, crash dump logs should be retrieved and decoded to ElasticSearch. |
| 16 | Remote debugging through ASD | System must be capable of doing remote debugging through a feature named ASD enabled in BMC FW. Besides, a VM/bare metal system working as a remote debugging console to collect error logs and to debug multiple SUTs in the cluster. |

**FTx Validation Test Exit Criteria**

Test exit is the milestone at which FTx validation officially concludes FTx testing. The exit milestone is marked by a readiness review and the declaration of FTx validation exit through the distribution of a FTx test exit report.

|  |  |  |
| --- | --- | --- |
| No. | Criteria | Description |
| 1 | All FTx testing completed | All test contents must be executed. No un-run or blocked test item remain. Expects to find all the FTx functionality and platform specific issues during each test phase. |
| 2 | Overall pass rate > 90% | In order to ensure that the overall system health is of sufficient quality, the pass rate must be over 90% |
| 3 | No Active Critical and High pre-sightings | In order to achieve test exit, all severity Critical and High pre-sightings must have been fixed and verified by the OxM. |
| 4 | All Medium and Low pre-sightings in Closed or verify states | All severity Medium and Low defects have been verified and closed. If any pre-sightings cannot be fixed timely, these pre-sightings must be root caused, with fixes identified. |
| 5 | Fixes of remaining pre-sightings scheduled for next test entry | The OxM shall have the pre-sighting fixes confirmed and delivered. If no next test cycle is planned, all pre-sightings must be resolved by test exit. |

# **FTx Validation Requirement**

This section provides the test overview of each test phase and the summary for each test contents that Intel requests.

## **Test Overview**

The test overview provides the high-level strategy and the reasons of why FTx validation program focuses on the specific test scope, and it acts as a baseline test of FTx validation program that helps OxM understand more detail to explore their own test contents.

**Phase1**

Phase1 of FTx Validation is a type of acceptance test suite run to ensure the SUTs are stable enough for following test contents. Phase1 consists of a set of Burn-in pipeline including cycling test, memory margin test and stress test for Intel silicon.

**Phase2**

Phase2 of FTx Validation is an extension test of Phase1 to ensure the SUTs’ silicon and I/Os stability with longer test duration on 2 test pipelines – Core Pipeline and Platform Content Pipeline that outline the various well-known stressors for CPUs, memories, storage devices and networking devices. The pass rate >90% must be met which is aligned with phase exit criteria. Otherwise, a regression test is required for pre-sightings fixing and verifying.

**Phase3**

Phase3 of FTx Validation includes elements of RAS, virtualization and security in order to ensure SUTs’ availability and reliability across different feature of CPU architectures. The purpose is to validate the specific test contents Intel defines work properly under various test methodologies. Each test content has particular test requirement, steps and criteria in follow sections.

**Extensive Phase**

Extensive Phase of FTx Validation is to perform hybrid test series. These series are like "assembly line" that OxM can reorder all the test contents and add additional well-known 3rd party test tools. Intel provides the reference pipelines named Combo1 to Combo5 for OxM executing to check whether the system works properly under system heavy load conditions. The OxM is responsible for completing all test pipelines Combo1 to Combo5 and providing the test concept, specific test content and test combination for their CSP customers based on what they’ve learned in FTx validation program from this phase.

The High-level concept of Extensive Phase is to:

* System level stress test with heavy loading by running various stress tools in-parallel
* Perform specific test contents with real-world scenarios from open source and proprietary tools
* Customized test contents by OxM
* Hybrid different stress ratio

## **Test Content Summary**

This section indicates the baseline test requirements of FTx validation Intel requests to help the OxM learn the test purpose, test scope and test procedures of each test content. The test methodologies and parameters can be adjusted depending on OxM’s product configuration and system specification after getting aligned with Intel ASV Team. For additional information on ASV Testing, please see the [FTx At-Scale Validation Test Content](https://intel.sharepoint.com/:w:/r/sites/asv-taiwan/Shared%20Documents/General/@scale%20validation%20plan/FTx%20At-Scale%20Validation%20Test%20Content%20v0.1.docx?d=wf805ab505d5949b1982bf0369979c711&csf=1&web=1&e=rUPtS7) document.

## **Baseline HW Material Requirement**

Intel ASV Team requests baseline quantity of SUT demand and minimum SUT configuration for FTx validation program. Since the OxM runs all the test contents in a cluster-scale environment through admin rack which is capable to handle 150+ SUTs running in-parallel, Intel ASV Team recommends the quantity of SUT should not be less than 50 units in order to find more specific pre-sightings in the FTx validation program.

**SUT Demand**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Phase1 | Phase2 | Phase3 | Extensive Phase |
| SUT Demand | >=50 | >=50 | >=50 | >=50 |

**Minimum Configuration Requirement**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| HW Material | | Phase1 | Phase2 | Phase3 | Extensive Phase |
| CPU | Stepping | >=ES1 | >=ES1 | >=ES1 | >=ES1 |
| Population | Full | Full | Full | Full |
| TDP | Highest | Highest | Highest | Highest |
| Core | - | - | Maximum | Maximum |
| Frequency | Highest | Highest | - | - |
| Memory | Population | >=1DPC | >=1DPC | >=1DPC | >=1DPC |
| Total Capacity | >=2GB per Core | >=2GB per Core | >=2GB per Core | >=2GB per Core |
| Frequency | Highest | Highest | Highest | Highest |
| Storage | NVMe – U.2 | 1 | 1 | 1 | 1 |
| NVMe – M.2 | 1 | 1 | 1 | 1 |
| PCIe Options | PCIe Gen | Highest | Highest | Highest | Highest |
| PCIe NIC | 1 | 1 | 1 | 1 |
| OCP NIC | 1 | 1 | 1 | 1 |

\*An SI corner case configuration list (High speed interface) and Phase Change List are required for reference.

\*The shipping configs of OxM’s customer must be considered first

## **FTx Validation Process**

### **Data Reporting**

In FTx validation, the OxM is responsible for collecting, summarizing and distributing below information to Intel Project Management Team and Intel ASV Team for test status alignment. The table provides an overview of the data reporting that the OxM monitors and provides.

|  |  |  |  |
| --- | --- | --- | --- |
| Report Type | Description | Timing | Format |
| OxM FTx Validation Status | The OxM provides weekly validation status including test execution progress, key pre-sightings, and highlights | Weekly | PPT |
| Test Plans | Summarizes the test content that need to be executed in next test phase | Test Entry -1 Week | OxM Defined |
| Test Reports | Summary of overall test status with pass rate | 100% Test Attempt | OxM Defined |
| Test Phase Entry Letter | The letter on the preparations for next FTx validation phase | Test Entry | E-mail |
| Test Phase Exit Letter | Summary of the test results, key sightings and highlights | Test Exit | E-mail |

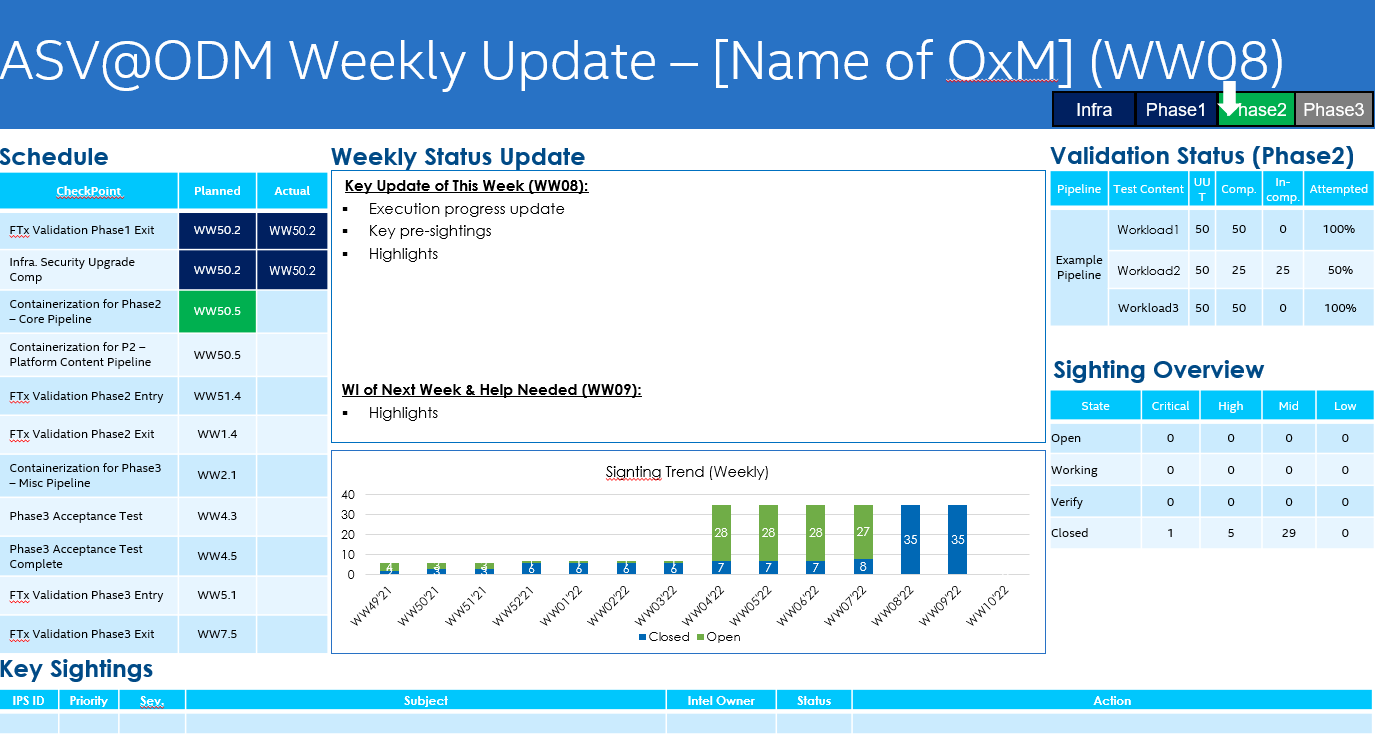
**OxM FTx Validation Status**

The regular updates of validation status must include below key information for alignment within Intel and the OxM.

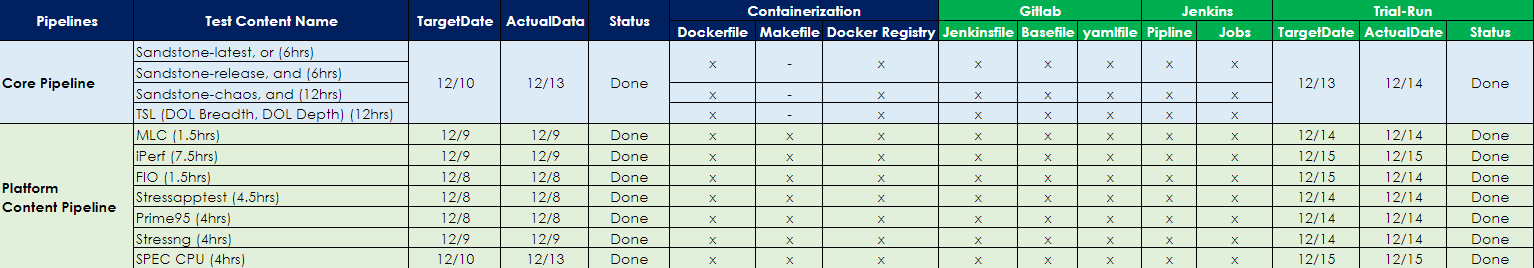
* Project Health: Green (On-track)/Yellow (Low Risk)/Red (Schedule behind)
* High-level Schedule
* Key Status Update with 3 key highlights affecting the program
* Validation Status with pass rate
* Sighting Overview, trend and highlighted key sightings

Given the examples of Validation Status Update as below:

* Weekly Update



* Preparation Checklist for test phases



**Test Plans**

The FTx Validation Test Plans combine Test Contents with specific system configurations to validate whole system stability and reliability through Intel At-Scale Validation test methods. The OxM is responsible for reviewing test requirements, raising questions and generating the test plans that cover all Intel defined test content from Phase1 to Phase3 as well as critical configuration. By following the [FTx test requirements](#_Test_Content_Overview), the test plans must include below key information as detailed as possible:

* Test Content Description
* Steps and Procedures
* Expected Results
* Time for Execution
* Pre-sighting ID
* The Name of Executor

Once test plans are created, the OxM needs to walk through the details with Intel ASV Team to get aligned the test contents are valid and executable.

**Test Reports**

During FTx validation, the OxM is responsible for driving the test execution to the defined schedule and logging pre-sightings to the tracking system, and the overall status is reported accurately in regular status updates. A summary test report is needed when test execution is completed, the test reports must include below key information based on the test plans provided in the beginning of each test phase entry:

* Test Passed/Failed/Blocked of each test item
* Overall pass rate
* Pre-sighting IDs, titles and links

**Test Phase Entry Letter**

Once all Test Entry criteria items achieves, the OxM needs to send out a letter of Phase Test Entry to declare test starting. The entry letter contains:

* List of Intel ASV Team and OxM contacts
* Configuration list of system under test
* Milestone
* Firmware level and BKC version for test entry
* [Test entry checklist](#_Appendices_C_–) with results
* List of approved exceptions and assumptions

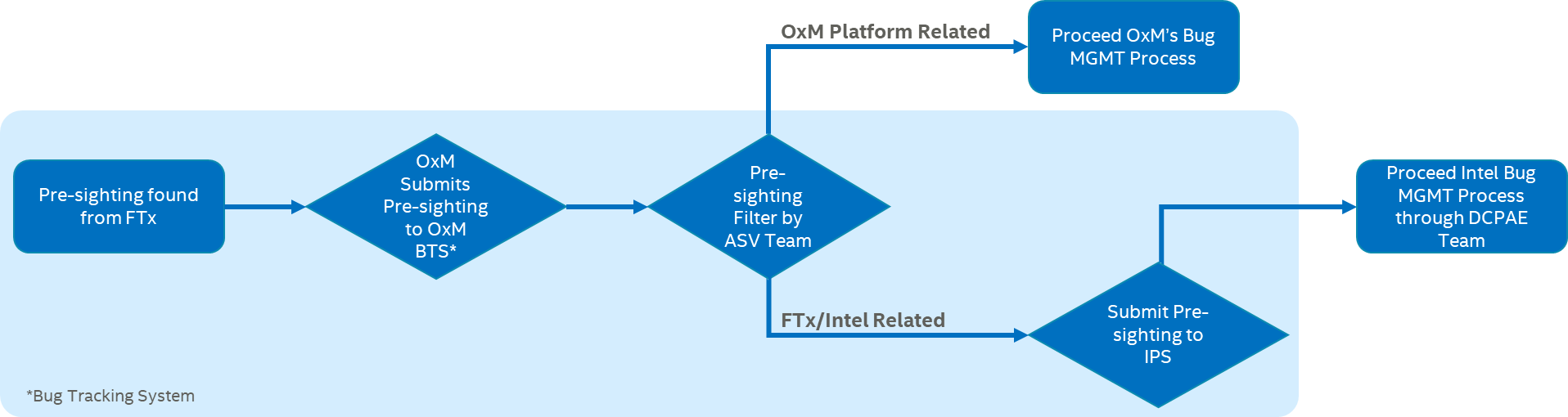
**Test Phase Exit Letter**

Once all Test Exit criteria items achieves, the OxM needs to send out a letter of phase Test Exit to declare test completion. The exit letter contains:

* List of Intel ASV Team and OxM contacts
* Configuration list of system under test
* Milestone
* Firmware level and BKC version for test exit
* [Test exit checklist](#_Appendices_C_–) with results
* List of approved exceptions

### **Pre-sighting Management Process**

Below flow chart indicates the pre-sighting process that the OxM has to follow in FTx validation program for pre-sightings’ submission, filtering and analysis.

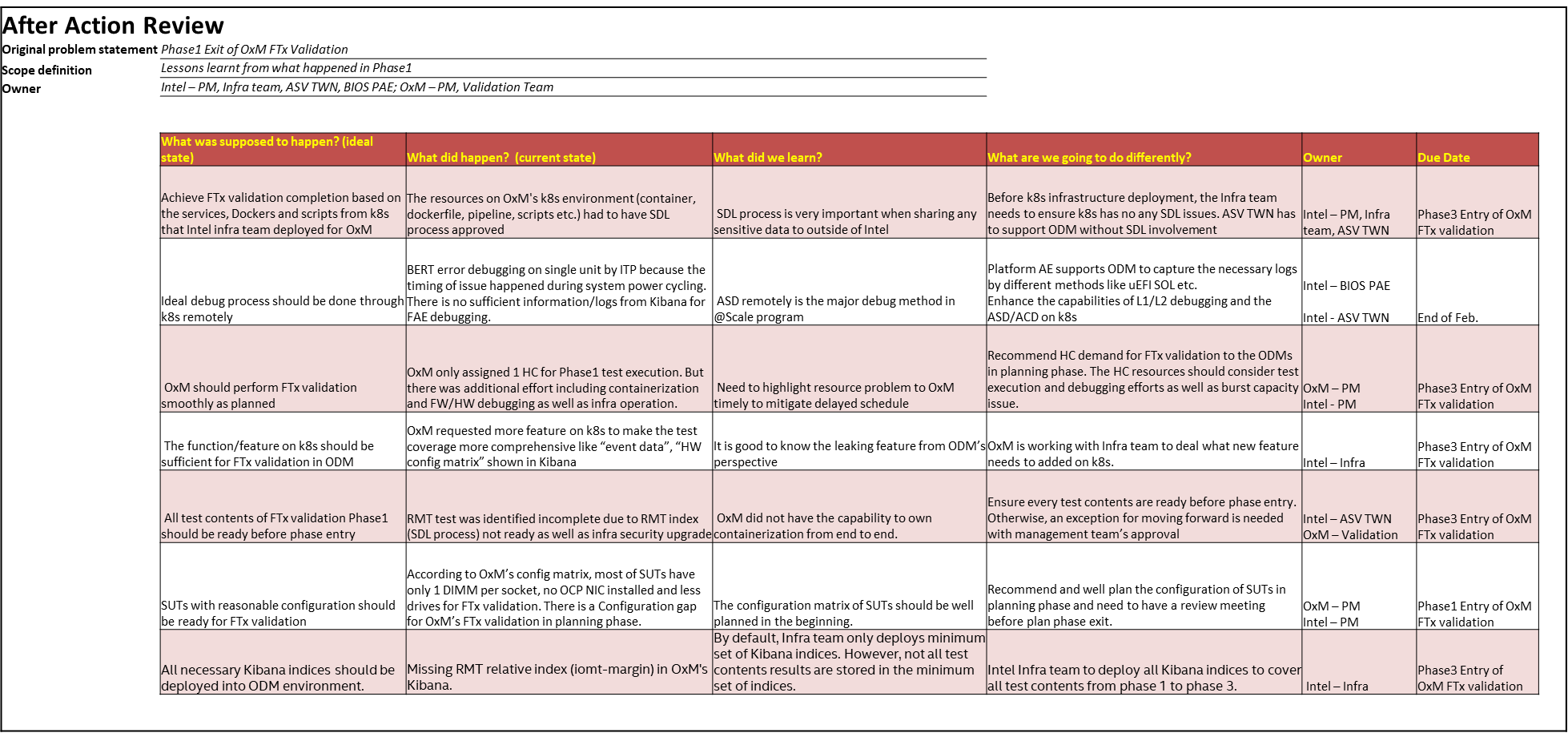


### **After Action Review (AAR)**

The After-Action Review (AAR) is the process of how Intel ASV Team/OxM analyses and documents process problems, design gaps and test escapes to implement corrective actions.

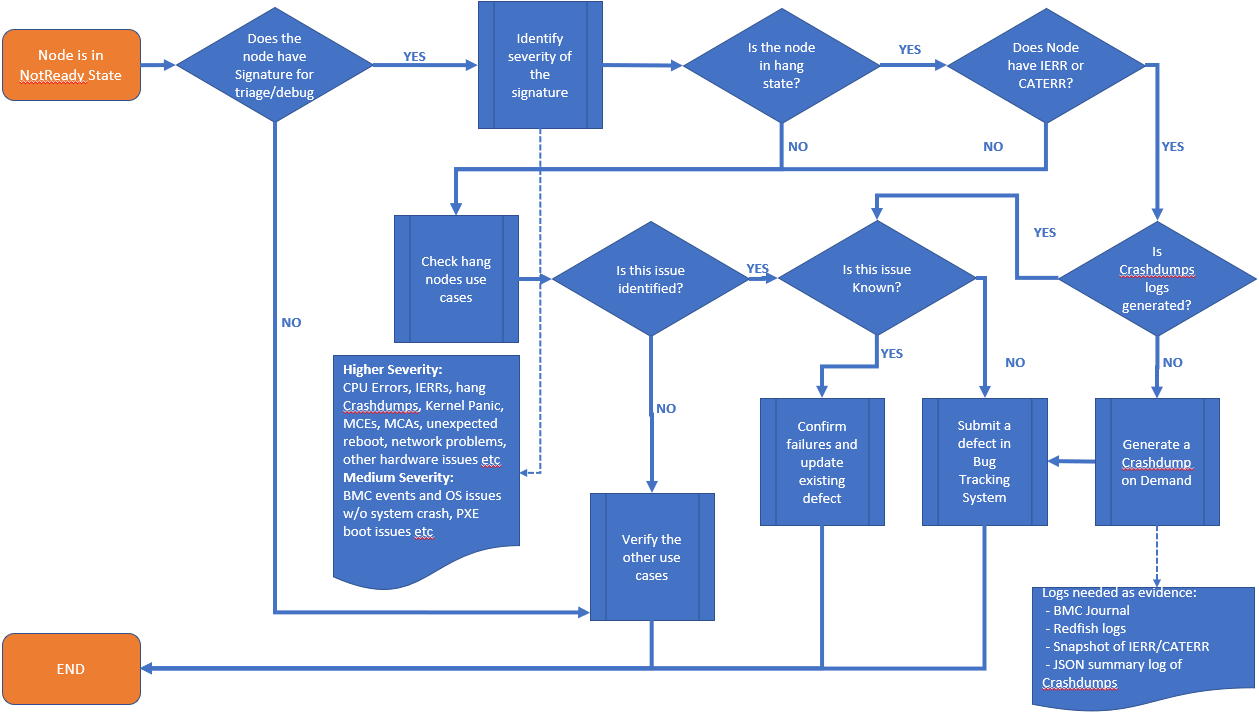
* Characterize the statement of problems à What was supposed to happen? (Ideal state)
* Define AAR scope à What did happen? (Current State)
* Identify the owner of AAR
* Identify root cause à What did we learn?
* Implement corrective actions à What are we going to do differently?
* Target date for AAR closure à Due date

Given an example of how to manage the AAR as below:



### **Triage and Debug Process**

This section indicates the process of triage and debug when a SUT is identified as NotReady in cluster and help the OxM to have a clear picture of how to process a problem in validation phase through ASV. Given the triage and debug flow as below that scope the whole triage/debug process to let OxM understand more detail.



Since there are 50+ SUTs in OxM’s ASV cluster, it is hard to perform debugging activities one by one on each NotReady nodes, the Intel ASV Team recommends to do triage/debug through the tools and methods under ASV environment. There are 5 steps supporting the OxM to do triage/debugging more convenient as well as make debug process more consistence.

Step1. Identify the NotReady nodes

Step2. Check system status and inventory

Step3. Crashdumps through CScripts

Step4. Check logs from Kibana/Grafana

Step5. Defect submission

**Step1. Identify the NotReady nodes**

A list of NotReady nodes w/ necessary information as below should be daily collected by debugger, it is helpful to let the developer to understand comprehensive situation of NotReady nodes and reduce the effort of back and force.

The explanation of each column:

|  |  |
| --- | --- |
| * Node – the node is in NotReady state | * Error Root Cause – the root cause of failure |
| * Content – Pipeline/pods in Jenkins | * Elastic logs – capture the failure logs from Elastic |
| * Reboot count – the times of reboot test, if applicable | * Crashdumps – the Crashdumps logs, if applicable |
| * Configuration – SUT configuration | * DefectID – the defect number if issue identified |
| * QDF – the CPU QDF | * Next step – the action, mitigation for next step |
| * Stepping – the CPU stepping |  |

**Step2. Check system status and inventory**

There are 2 recommended ways to check current system status

* BMC Web GUI
  + KVM
  + SOL
  + Eventlogs
  + Download Crashdumps from BMC web GUI
* SSH
  + dmeag
  + networking status
  + kernel messages
  + MCE/MCA logs

**Step3. Crashdumps through CScripts**

Generate Crashdumps by using CScripts commands (if applicable).

1. Run command to activate CScripts to ensure CScripts venv is activated

activate\_cscripts

1. Run CScripts command to launch CScripts

lanch\_cscripts <node\_name>

1. Run CScripts command to generate Crashdumps logs
   * Error.crashdump()

*WARNING: Crashdump big\_core(Core GP regs and Core-MCA) collection is disabled, make sure to Disable CPU crashlog from BIOS options*

*!! Unable to determine PCI MMCFG base address while ITP is running*

*!! for most scripts to work you will need to 'halt()', then run 'initpci()' before proceeding*

*Conditions are met to use accelerated crashdump...*

*Please wait...*

*------------Elapsed Time: 197.8907549381256 seconds ----------------crashdump() log file created at: C:\Users\lab\_pcsdpvl\PythonSv\crashdump\_20220511\_183543.json>>> error.crashdump\_summary(r'C:\Users\lab\_pcsdpvl\PythonSv\crashdump\_20220511\_195112.json')*

*Output file location and Operating on Directory tree here: C:\Users\lab\_pcsdpvl\PythonSv*

*\* Found SPR project file crashdump\_20220511\_183543.json*

*+ Processing crashdump file: C:\Users\lab\_pcsdpvl\PythonSv\crashdump\_20220511\_183543.json*

*=> Output summary file: summary\_crashdump\_20220511\_183543.txt*

* + error.dumpAll()

**Step4. Check logs from Kibana/Grafana**

* Indexes need to be checked on Kibana
  + qpool – status of test runs
  + sol\_raw – logs under operating systems
  + Eventlog\_raw – BMC eventlogs raw data
  + Crashdumps – triggered by critical events
  + failures – failures found according to error keywords in [Appendices D](#_Appendices_D_–)
  + tests – status of test runs
* Grafana (optional) – checking for system HW health
* Some recommended keywords that need to be queried in Kibana/Elastic, check [Appendices D](#_Appendices_D_–) for more detail.

**Step5. Defect submission**

In general, defect found from FTx validation should go through the OxM defect process. The OxM is responsible for the defects’ submission with comprehensive information and well management in order to provide valuable and qualified defects to the developers of each function owner for further debugging. Here is the minimum requirement that need to be considered when submitting a defect.

Title

The information of title requires failed function, error type, node name and high-level description. Given an example as below.

[Function\_Impacted][Error\_Type][Node\_Name]Short\_Description

[BMC][Thermal Trip][a001s001]CPU0 Thermal Trip Occurred during CPU Stress Test

Description

Describe the failed node behaviour as detail as possible and the status when errors found. Completed logs and commands related to the errors should be provided as well.

Logs and Attachments

The defect submitter is responsible for collect below logs from Kibana/Elastic and attach them to BTS.

* Qpool – test run w/ errors – the logs corresponding to latest test run
* Sol\_raw – SOL logs – the logs corresponding to latest test run
* Eventlog\_raw – BMC event logs – the logs corresponding to BMC event of latest test run
* Crashdumps – the logs corresponding to Crashdump logs when IERR/CATERR/MCE/MCA bank occurred

Qpool timeline

The lines of qpool logs with the latest executed test.

SOL logs (last)

The lines of qpool logs with the latest executed test.

System configuration

Follow OxM configuration format is the minimum requirement.

# **Appendices A – Terminology**

|  |  |  |  |
| --- | --- | --- | --- |
| **Term** | **Definition** | **Term** | **Definition** |
| AAR | After Action Review | OOB | Out of Band |
| AMT | Advance Memtest | OxM | Original Design/Equipment Manufacturers |
| ASV | At-Scale Validation | PO | Power On |
| BDAT | BIOS Data Area Table | RAS | Reliability, Availability, Serviceability |
| BIOS | Basic Input Output System | RMT | Rank Margin Tool |
| BMC | Baseboard Management Controller | R&R | Role & Responsibility |
| CSP | Cloud Service Provider | SHC | System Health Check |
| DC | Direct Current | SI | Signal Integrity |
| FISHER | Fault Injection Software Hook | SME | Subject Matter Expert |
| FTx | Fast Track | SOL | Serial Over LAN |
| IB | In-band | SPR | Sapphire Rapid |
| ICX | Ice Lake | SUT | System Under Test |
| IPSS | Intel® Post-Silicon Services | 1DPC | 1 DIMM Per Channel |
| LLD | Low-Level Data Gathering Tool |  |  |

# **Appendices B – Pre-sighting Severity Definition**

|  |  |  |
| --- | --- | --- |
| **Severity** | **Failure Signature** | **Action** |
| Critical | * Program level impact (PO, TI, ES, PRQ..) * Break key functionality, a quality criteria w/o workaround * Blocks validation * High customer visibility | Daily intensive work, daily sighting updates. Kick-off TF if required. Get all the resources needed (HW/SW, support) |
| High | * Key functionality, multiple configurations, product not reliably usable * Blocks some areas of validation * Should be root caused and addressed before next program milestone | Daily attention, daily sighting updates. |
| Medium | * Visibility across configuration, low customer visibility * Easy, low impact workaround * Medium impact on validation, functionality, or power | Weekly attention, weekly sighting updates. |
| Low | * No impact to product quality * Tolerable impact to validation, functionality or power * Does not meet any of the criteria for other priority levels |  |

# **Appendices C – FTx Validation Entry/Exit Criteria Checklist Template**

**FTx Validation Test Entry Criteria**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **No.** | **Criteria** | **Description** | **Achieved** | **Remark** |
| 1 | Cluster Power On | All tasks completed per power on plan or infrastructure readiness plan. Systems delivered and proven capable to execute orchestrated validation execution and telemetry functionality meets expected tracking and monitoring requirements per failure criteria | Y |  |
| 2 | Platform BKC | Alignment with platform BKC is completed. BKC transitions happen on all external releases (minimum requirement). Specific ingredient transitions in off-cycle mode are possible upon agreement with platform and BKC team to ensure risks are understood | Y | Latest BKC version: WWxx Latest BIOS version: xxxxxx Latest BMC version: xxxxxx |
| 3 | Silicon availability | Cluster infrastructure team has plans to enable minimum counts of CPUs necessary to cover HW and platform milestones per product life cycle documentation and validation plan schedule. Item tracked as part of cluster power on milestones. | Y | CPU stepping: D0/ES1/ES2/QS PCH stepping: xxxxxx |
| 4 | Content quality and execution method | Content must meet stability requirements per the power on phases. All content execution is completed with automated orchestration and meets ‘Test Anything Protocol’ to ensure telemetry is integrated into the test pass/fail monitors. | Y |  |
| 5 | Cluster fleet stability | Calculation methods and tools for stability assessments are ready on first validation cycle and minimum failure criteria exists and meets the expected minimum measurement required for first UPLC criteria, i.e. component ES2 and/or Platform Beta. | Y |  |
| 6 | Telemetry readiness | Proof of readiness is demonstrated at minimum against n-1 technology, i.e. reference SPR/EGS telemetry must have at least the same capabilities are those that currently exist in Whitley platform. Especially the path of uEFI debug logs through SOL (Serial-Over-LAN) and sensor list (via IPMI/Redfish) need to be feature completed and validated by the OxM. | N | Some data of cycling counts dropped from Kibana but Jenkins. Exception approved by xxxxxx. |
| 7 | OxM's SIT test report and known issues availability | OxM's SIT test should be completed and results should be reported prior to FTx Validation Entry. Any known pre-sightings will have been recorded for the product. Any pre-sightings that will not be resolved prior to test Entry must have been reviewed to ensure they will not block FTx testing. An SI corner case configuration list (High speed interface) is required as well. | Y |  |
| 8 | OxM's product is at least DVT level (HW & FW) | The FW and HW features of OxM’s product must be DVT level (HW feature enablement completed) at least and have been tested prior to test Entry. | N | FW feature is not completed |
| 9 | Materials (UUTs, test tools) readiness | OxM's lab infrastructure, configuration of test Systems and components, and test tools must all be available prior to test entry. | Y |  |
| 10 | Manpower readiness | All planned execution personnel must be available. All required training Intel provided for the project should be completed before test entry. | Y |  |
| 11 | Acceptance test 100% passed | OxM will perform a set of ASV team defined acceptance tests to ensure that the systems and infrastructure are ready for test entry. Results with 100% passed will be provided to Intel ASV team prior to test entry. | N | Acceptance test is not completed |
| 12 | All test plans ready and reviewed | The test Plans must be finalized and reviewed prior to test entry. | N | Target release date on WW xx.x |
| 13 | OxM’s pre-sighting list is provided and reviewed | OxM must provide the defect list to ASV team for reviewing to ensure no potential rick gating FTx validation progress prior to test entry. | Y |  |
| 14 | Data analytics readiness | 1. OxM must maintain the correctness of data and logs inside the following indices.    1. qpool-\* (In-band logs)    2. sol-\* (OOB logs)    3. eventlog-\* (BMC event logs)    4. crachdumps-\* (Crachdumps logs)    5. other relevant indices 2. OxM must maintain the correctness of [Appendices D](#_Appendices_D_–). 3. OxM must label the status of the SUT according to the status of the tests. (Execution, Debug, etc.) |  |  |

**FTx Validation Test Exit Criteria**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **No.** | **Criteria** | **Description** | **Achieved** | **Remark** |
| 1 | All FTx testing completed | All test contents must be executed. No un-run or blocked test item remain. Expects to find all the FTx functionality and platform specific issues during each test phase. | Y |  |
| 2 | Overall pass rate > 90% | In order to ensure that the overall system health is of sufficient quality, the pass rate must be over 90% | Y |  |
| 3 | No Active Critical and High pre-sightings | In order to achieve test exit, all severity Critical and High pre-sightings must have been fixed and verified by the OxM. | Y |  |
| 4 | All Medium and Low pre-sightings in Closed or verify states | All severity Medium and Low defects have been verified and closed. If any pre-sightings cannot be fixed timely, these pre-sightings must be root caused, with fixes identified. | N | 1 minor pre-sighting ID\_xxxxxx has been root caused and will be fixed in next release which is not gating phase exit. |
| 5 | Fixes of remaining pre-sightings scheduled for next test entry | The OxM shall have the pre-sighting fixes confirmed and delivered. If no next test cycle is planned, all pre-sightings must be resolved by test exit. | Y |  |

# **Appendices D – Keyword to query from Kibana/Elastic**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Index to query | Field to query | Keyword | Fail type | Component | Critical failure |
| sol-\* | message | kernel panic | Kernel Panic | Software | Yes |
| sol-\* | message | rebooting in 10 seconds | Reboot | Software | Yes |
| sol-\* | message | Corrected error | Corrected HW | PCIe | No |
| sol-\* | message | machine check bank | MCE | CPU | No |
| sol-\* | message | [Mca]McBankErrorHandler:, MC status | MCE Without Reboot | CPU | No |
| sol-\* | message | Failure detected - | UCE MemTest | Memory | Yes |
| sol-\* | message | UPI: LL Rx detected CRC error | UPI | UPI | Yes |
| sol-\* | message | [WheaBERT] CheckAndUpdatePrevBootErrors: | WHEABERT | Hardware | Yes |
| qpool-\* | message | EDAC | EDAC | Firmware | Yes |
| sol-\* | message | \*\*ERROR! PCODE | Pcode | Power | Yes |
| sol-\* | message | PCIe error | PCIe | PCIe | No |
| sol-\* | message | Hardware error from APEI Generic Hardware Error Source | APEI | Hardware | No |
| sol-\* | message | general processor error | Processor | CPU | No |
| sol-\* | message | error overflow | Overflow | CPU | No |
| sol-\* | message | uncorrected error | Uncorrected HW | Hardware | No |
| sol-\* | message | [Hardware Error]: DIMM location | DIMM | Memory | No |
| sol-\* | message | uma read integrity error | UMA | CPU | No |
| sol-\* | message | UMA Read/Write timeout | UMA | CPU | No |
| sol-\* | message | PXE boot failed! | PXE Boot | Firmware | No |
| sol-\* | message | Find imaged based on IP | Find Image IP | Firmware | No |
| sol-\* | message | blk\_update\_request: I/O error | IO Error | Hardware | No |
| sol-\* | message | nvme nvme0: controller is down | Controller Down | Hardware | No |
| sol-\* | message | [Hardware Error]: command: | Hardware Error Command | Hardware | No |
| sol-\* | message | [Hardware Error]: It has been corrected by h/w and requires no further action | Correctable Error | Hardware | No |
| sol-\* | message | [Hardware Error]: event severity: corrected | Correctable Error | Hardware | No |
| sol-\* | message | [Hardware Error]: Error 0, type: corrected | Correctable Error | Hardware | No |
| sol-\* | message | [Hardware Error]: fru\_text: | Correctable Error | Hardware | No |
| sol-\* | message | [Hardware Error]: section\_type: memory error | Correctable Error | Hardware | No |
| sol-\* | message | [Hardware Error]: error\_status: 0x0000000000000400 | Correctable Error | Hardware | No |
| sol-\* | message | [Hardware Error]: physical\_address: | Correctable Error | Hardware | No |
| sol-\* | message | [Hardware Error]: node: | Correctable Error | Hardware | No |
| sol-\* | message | [Hardware Error]: error\_type: 2, single-bit ECC | Correctable Error | Hardware | No |
| sol-\* | message | [Hardware Error]: DIMM location: | Correctable Error | Hardware | No |
| sol-\* | message | PMIC Enable Failure: | SM Bus | Memory | No |
| sol-\* | message | Apply 1.2V VDDIO Failure: | SM Bus | Memory | No |
| sol-\* | message | PPR resource not available | CE MemTest | Memory | Yes |
| sol-\* | message | Error on rising strobe: | CE MemTest | Memory | Yes |
| sol-\* | message | RC\_FATAL\_ERROR! | MemTest | CE Memory | Yes |
| sol-\* | message | Adv MemTest Reset Failure | MemTest | Memory | Yes |
| sol-\* | message | Major Warning Code | UCE Mem Interface | Memory | No |
| sol-\* | message | Minor Warning Code | UCE Mem Interface | Memory | No |
| sol-\* | message | Major Checkpoint | UCE Mem Interface | Memory | No |
| sol-\* | message | Minor Checkpoint | UCE Mem Interface | Memory | No |
| sol-\* | message | DisableRank() | CE Mem Interface | Memory | No |
| sol-\* | message | CheckMemoryBootError | CE Mem Interface | Memory | No |
| sol-\* | message | Active Memory | Inconsistent Memory Error | Memory | No |
| qpool-\* | log | not ok | Not Ok | Software | No |
| qpool-\* | log | TSC warp | TSC Counter | Software | Yes |
| qpool-\* | log | TSC unstable | TSC Counter | Software | Yes |
| qpool-\* | log | downgraded | Downgraded | PCIe | Yes |
| qpool-\* | log | coredump | Coredump | Software | Yes |
| qpool-\* | log | Mismatch detected in | DTAF\_UPI | UPI | No |
| qpool-\* | log | Root Port Correctable errors, Endpoint Uncorrectables,  Endpoint Correctables,  Recoveries detected,  Enabling ASPM L1,  checking for L1... failed,  removing port from test | DTAF\_PCIe | PCIe | No |
| qpool-\* | log | FailMask | Not Ok | Software | No |
| eventlog-\* | message | IERR | IERR | CPU | Yes |
| eventlog-\* | event.severity | Critical | BMC Critical Event | Firmware | Yes |
|  |  |  |  |  |  |
| eventlog-\* | event.messageid | OpenBMC.0.1.ServiceFailure | OpenBMC Service Failure | Firmware,BMC | No |
| bmcjournal-\* | message | rcu\_sched self-detected stall on CPU | BMC RCU Stall | Firmware | No |
| crashdumps-\* | \* | \* | Crashdump | CPU | Yes |